The Boeing Company
900 N. Sepulveda Blvd.
El Segundo, CA 90245

07 September 2010
ES-3100-DM-10-163

To: Office of Naval Research
875 North Randolph Street, Suite 1425
Arlington, VA 22203-1995

Attn: Deborah Van Vechten, Program Officer

Subject: Purchase Order N00014-09-M-0052 for Superconductive ADC Project;
Delivery of CDRL # 0001AD – "Final Design Review Package"

Please accept the included file as delivery of CDRL No. 0001AD "Final Design Review Package."

If you have any inquires or need further clarification regarding this correspondence, please contact Dan Medina at 310.364.5432, or daniel.n.medina@boeing.com.

Sincerely,

Marcus Cooke
Manager of Contracts
Compliance and Contract Operations
Space and Intelligence Systems

CC: Anthony Tysenn, ONR Contracts Specialist
Judy Whalen, Administrative Contracting Officer (transmittal letter only)
Director, Naval Research Lab (hardcopy mailed)
Eva Adams/Shari Pitts, Defense Technical Information Center
Brad Perranoski, Boeing Principal Investigator
Dan Medina, Boeing Contracts Administrator

REPORT DOCUMENTATION PAGE

Form Approved
OMB No. 0704-0188

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07-09-2010	Final	16 March 2009 - 07 September 2010

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CDRL 0001AD Final Design Review Package (Fabrication Package)

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5b. GRANT NUMBER

5c. PROGRAM ELEMENT NUMBER

6. AUTHOR(S)

Perranoski, Brad S

5d. PROJECT NUMBER

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5f. WORK UNIT NUMBER

7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES)

The Boeing Company, through its wholly-owned subsidiary, Boeing Satellite Systems, Inc.
900 N Sepulveda Blvd.
El Segundo, CA 90245

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ONR SCADC CDRL 0001AD

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13. SUPPLEMENTARY NOTES

14. ABSTRACT

This project involves collaboration between industry (Boeing & Hypres) to examine the potentials of superconductive electronic (SCE) technology for the realization of a radio frequency (RF) analog to digital converter (ADC) that will meet the rigorous requirements of a direct RF to digital receiver intended for communication applications. Software defined radio (SDR) systems will use this device to enhance system performance and provide reconfigurable features. Superconductive electronic (SCE) technology possesses a set of characteristics uniquely suitable for the implementation of analog to digital conversion and digital signal processing (DSP) circuitry. This technology incorporates especially high switching speed, ultra low power, natural quantization, quantum accuracy, high sensitivity, superior filter performance, and low thermal noise. Both military and commercial communication applications will benefit immensely from a flexible, reconfigurable, multi-standard, multi-mode, multi-band communication system.

15. SUBJECT TERMS

ADC - Analog to Digital Converter, DSP- Digital Signal Processing, Direct RF to Digital Receiver, SDR - Software Defined Radio, SDC - SuperConductive Electronics.

16. SECURITY CLASSIFICATION OF:			17. LIMITATION OF ABSTRACT	18. NUMBER OF PAGES	19a. NAME OF RESPONSIBLE PERSON
a. REPORT	b. ABSTRACT	c. THIS PAGE			Daniel N Medina
U	U	U	UU	29	19b. TELEPHONE NUMBER *(Include area code)* 310-364-5432

ONR SCADC
Final Design Review Package

Superconductive ADC Project

Fabrication Package

Brad Perranoski

Engineer/Scientist, Boeing

(brad.s.perranoski@boeing.com)

Outline

1. Recap of Previous Design Reviews
2. Current Project Schedule
3. Modulator Design Documentation
   a. Modulator System Analysis (Simulink FFT)
   b. Simulated vs Tested Performance
   c. Performance Summary
   d. Resonator Implementation (Schematic & Simulation Results)
   e. Clock Driver Design (Schematic & Simulation Results)
   f. Comparator Design (Schematic & Simulation Results)
   g. DFF Design (Schematics)
   h. 2nd Order Bandpass Design (Schematics & Simulation Results)
   i. Potential ENOB Improvements
4. Conclusion
   a. What was done on this project:
   b. We did not meet the goals of this project because:
   c. This is where we are:

Recap of Previous Design Reviews Introduction

This Design Review Package is the fourth and final of four deliverables required by the contract/purchase order N0: N00014-09-M-0052 from the Office of Naval Research to Boeing.

The goal of this project is to:

1. **Improve the performance (ENOB) of an existing Hypres X-band delta sigma ADC modulator design that was tested during initial testing phase of this project through circuit design techniques, process improvements, and architectural enhancements.**
2. **Discuss the theory behind the improvements that were made providing analyses of critical enhancements.**
3. **Document the evolution of the design**
4. **Provide insight into further improvements that may potentially increase the ENOB performance.**

Recap of Previous Design Reviews
Previous Performance Summary

Based on high level Matlab simulations the analyzed ADC performance is captured below:

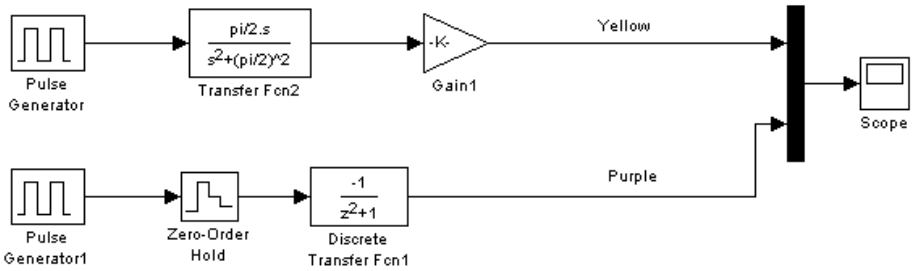
Category			X band RF to Digital ADC		High Level Matlab Simulation	
Item #	ADC Requirement	Units	Project Specification	Project Goal	2nd Order Design	4th Order Design
1	Center Freq. (f_{in})	GHz	7.30	7.30	7.50	7.50
2	Sampling Frequency (Fs, clk)	GHz	30.00	60.00	30.00	30.00
3	Bandwidth (BW)	MHz	58.59	117.19	58.59	58.59
4	Over Sampling Ratio (OSR)		256	256	256	256
5	Physical Bits	bits	1	1	1	1
6	ENOB	bits	7.74	10	10.42	16.17
7	Signal to Integrated Noise And Distortion (SINAD)	dBFS	48.35	61.96	------	------
8	Spurs. Free Dynamic Range (SFDR)	dBFS	60	70	------	------
9	Signal to Quantization Noise (SQNR)	dBFS	58.35	71.96	64.50	99.10

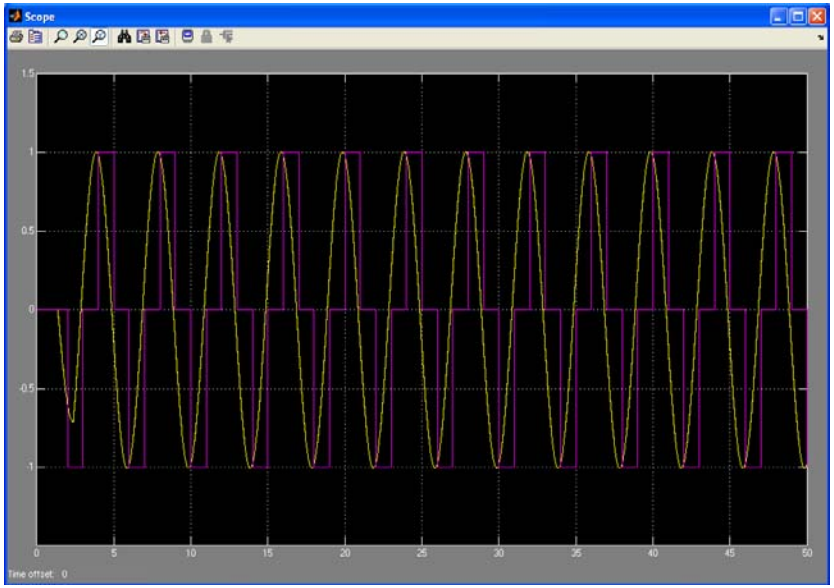
- **The Matlab simulations predict the expected performance is well above the project specification.**
- **The analysis is based on an ideal system and only considers quantization noise, however, it does provide a level of confidence that the improvements can be met with this approach.**

Recap of Previous Design Reviews
Modulator Transient Simulation
Z-domain vs S-Domain

Initial Simulink Simulation

- Loop Filter Transfer function Matlab/Simulink Simulation (2nd Order Bandpass)





Simulink Analysis Schematic

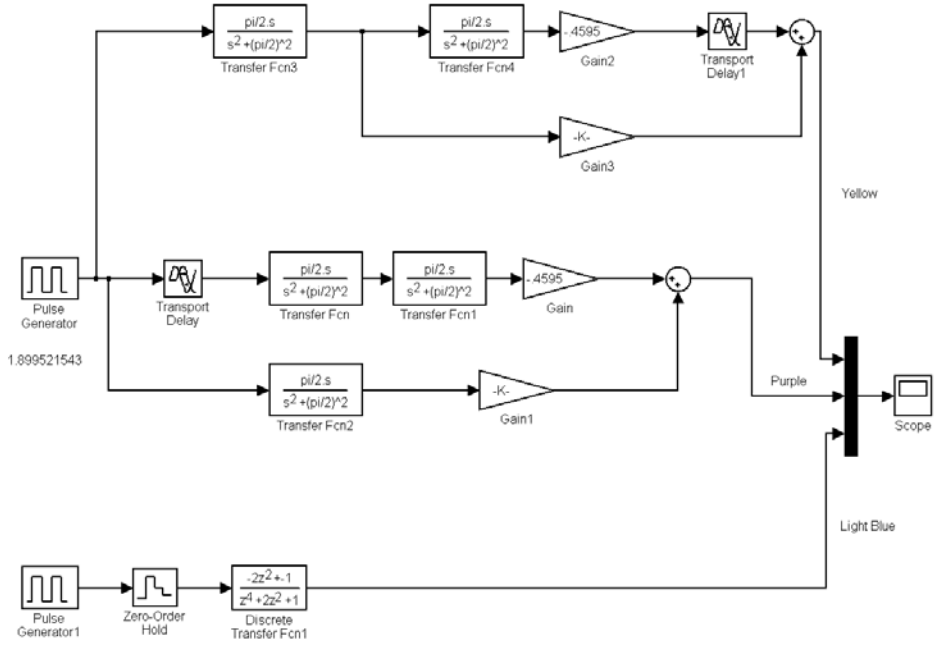
Simulink Transient Analysis Results

- **The Z-domain loop filter transfer function matches both S-domain transfer functions**
- **This is my initial cut at the Simulink Analysis (further analysis is needed)**

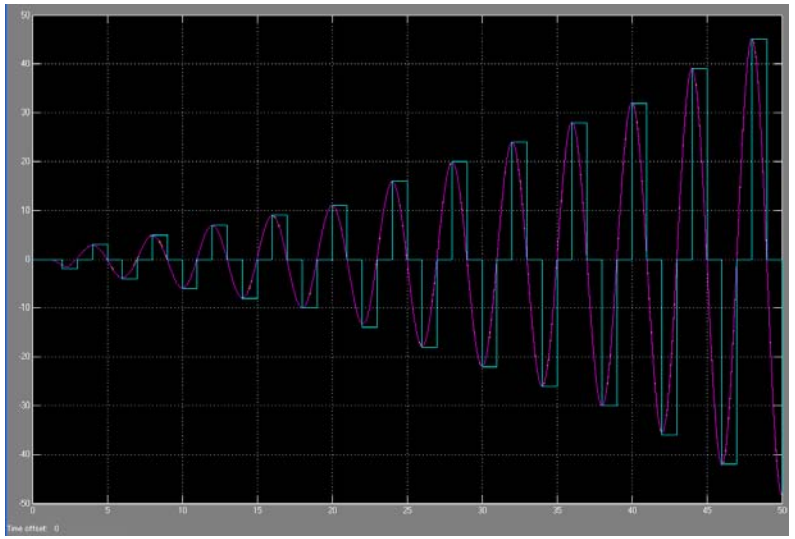
Recap of Previous Design Reviews
Modulator Transient Simulation
Z-domain vs S-Domain

Initial Simulink Simulation

- Loop Filter Transfer function Matlab/Simulink Simulation (4th Order Bandpass)



Simulink Analysis Schematic



Simulink Transient Analysis Results

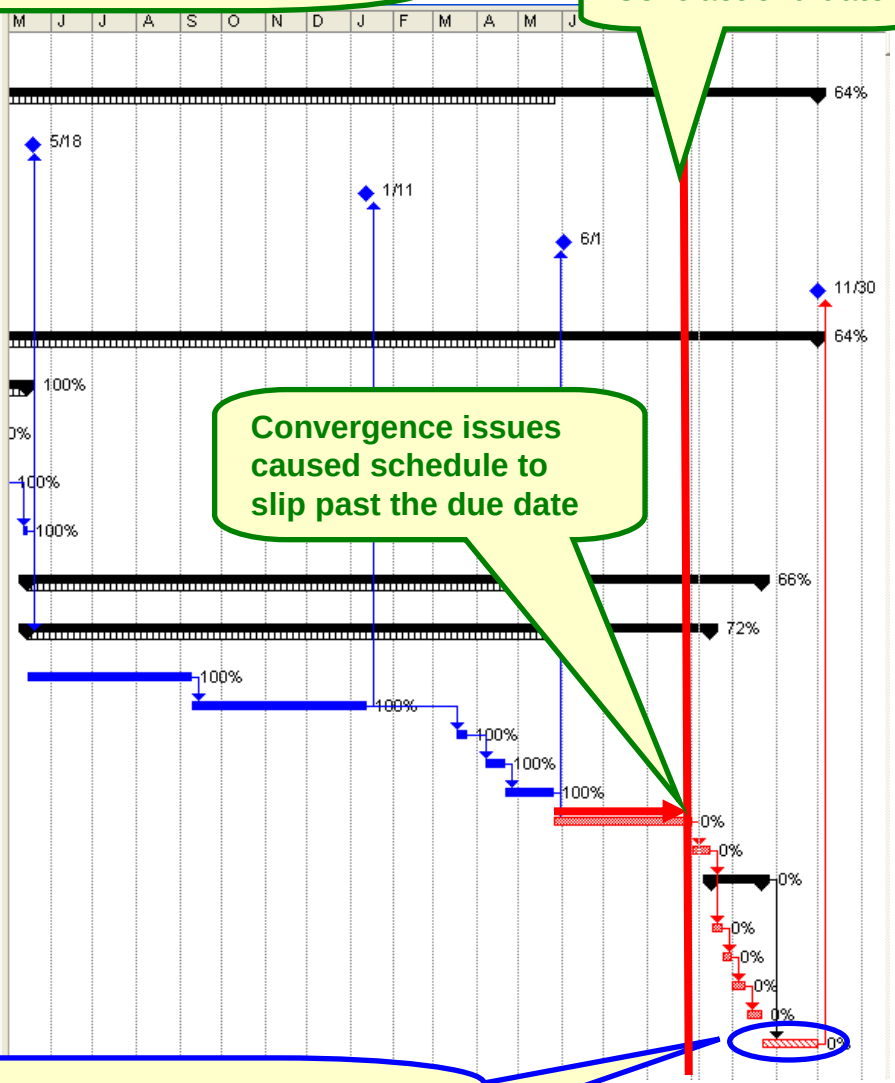
- **The Z-domain loop filter transfer function matches both S-domain transfer functions**
- **This is my initial cut at the Simulink Analysis (further analysis is needed)**

Current Project Schedule

The Fabrication Package
Behind Schedule: DFF was unable to be simulated due to convergence errors schedule slip

Contract end date

	Task Name	Duration	Start	Finish
1	Start	0 days	Mon 3/16/09	Mon 3/16/09
2	**Superconductive ADC Effort**	**435 days**	**Mon 3/16/09**	**Tue 11/30/10**
3	Test Data Review (ONR Milestone)	0 days	Mon 5/18/09	Mon 5/18/09
4	Design Review (ONR Milestone)	0 days	Mon 1/11/10	Mon 1/11/10
5	Final Design Review (ONR Milestone)	0 days	Tue 6/1/10	Tue 6/1/10
6	Fabrication Report	0 days	Tue 11/30/10	Tue 11/30/10
7	**1st Phase Test & Design (ONR)**	**435 days**	**Mon 3/16/09**	**Tue 11/30/10**
8	**Test & Evaluation**	**44 days**	**Mon 3/16/09**	**Thu 5/14/09**
9	Test Plan	20 days	Mon 3/16/09	Fri 4/10/09
10	Testing (at Hypres)	10 days	Mon 4/20/09	Fri 5/1/09
11	Data Evaluation	4 days	Mon 5/11/09	Thu 5/14/09
12	**Design Phase**	**362 days**	**Fri 5/15/09**	**Wed 10/20/10**
13	**Design & Schematic Capture (ADC Design)**	**335 days**	**Fri 5/15/09**	**Mon 9/13/10**
14	Loop Filter TF Design (Matlab)	80 days	Fri 5/15/09	Tue 9/8/09
15	Loop Filter Verification (Simulink)	80 days	Wed 9/9/09	Mon 1/11/10
16	Modulator Arch Design (Simulink)	6 days	Wed 3/17/10	Wed 3/24/10
17	Resonator Implem. (Schematic)	10 days	Wed 4/7/10	Tue 4/20/10
18	Comp Design (Schematic)	25 days	Wed 4/21/10	Tue 5/25/10
19	DFF Design (Schematic)	70 days	Wed 5/26/10	Tue 8/31/10
20	Modulator Design (Schematic)	9 days	Wed 9/1/10	Mon 9/13/10
21	**Layout**	**25 days**	**Thu 9/16/10**	**Wed 10/20/10**
22	Initial Layout	5 days	Thu 9/16/10	Wed 9/22/10
23	Simulation Verification	5 days	Thu 9/23/10	Wed 9/29/10
24	Optimized Layout	7 days	Thu 9/30/10	Fri 10/8/10
25	Simulation Verification	8 days	Mon 10/11/10	Wed 10/20/10
26	**Fabrication**	29 days	Thu 10/21/10	Tue 11/30/10



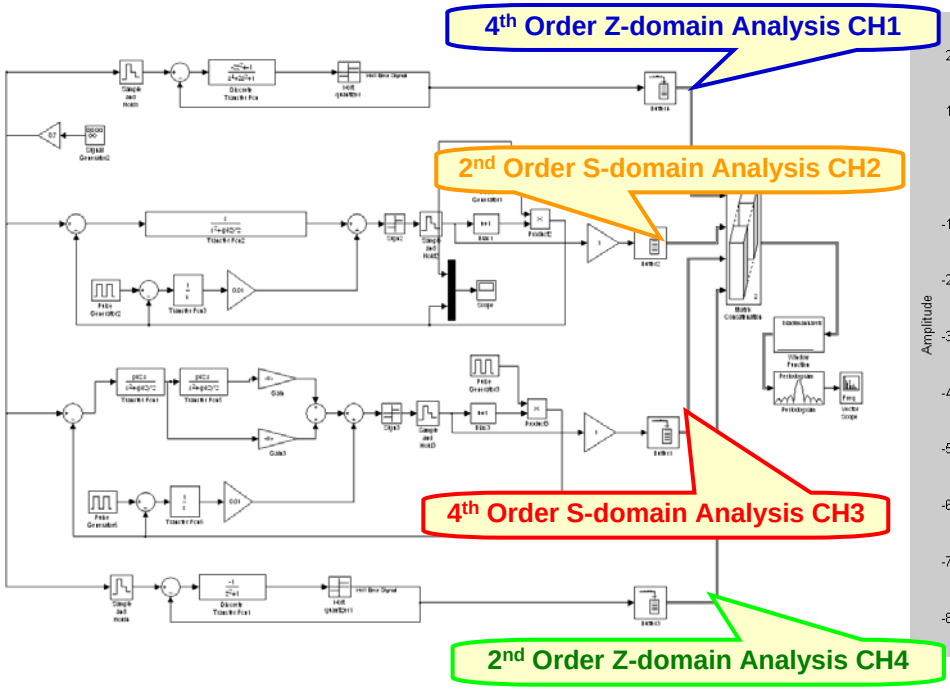
Convergence issues caused schedule to slip past the due date

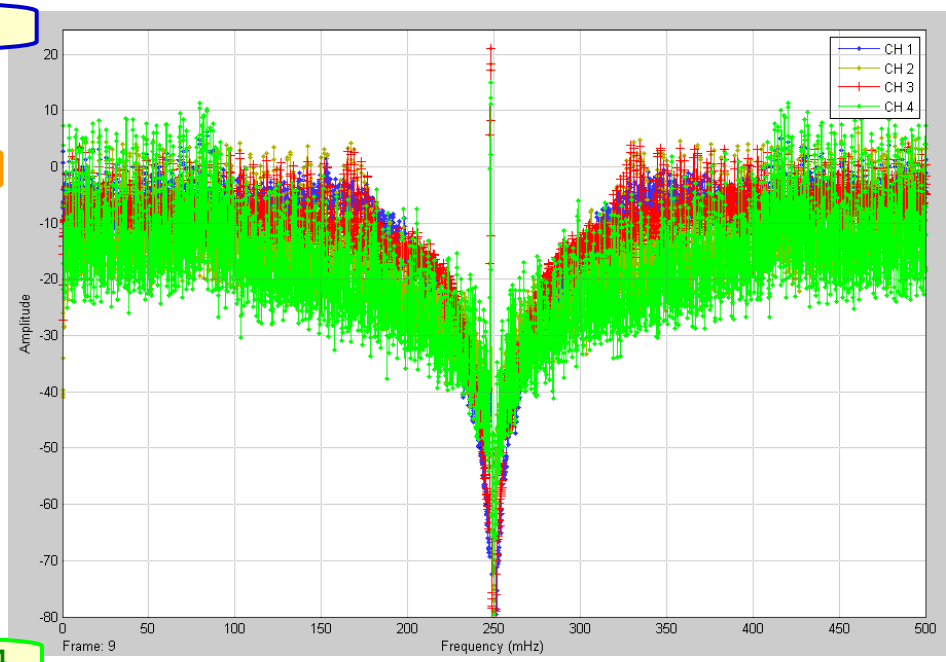
Boeing recommends that the fabrication task not be performed because neither the design goal has not been met nor the capability improvement is mutually considered significant (as stated in the SOW)

Modulator Design Documentation
System Analysis

Simulink Frequency Domain Simulation Analysis

Modulator Matlab/Simulink Simulation (2nd & 4th Order Bandpass)





Simulink Analysis Schematic

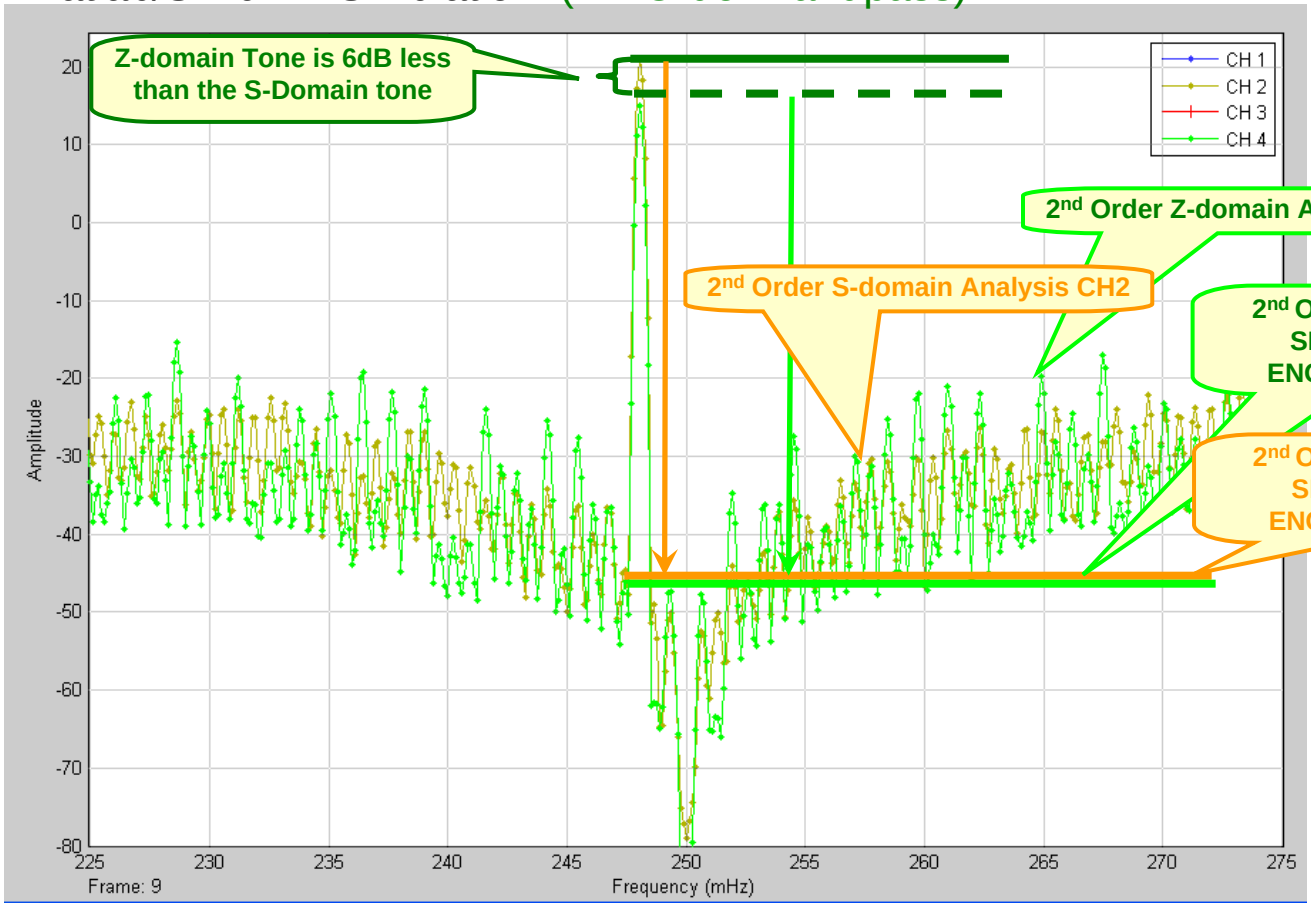
Simulink FFT Analysis Results

- **The Z-domain loop filter transfer function matches S-domain transfer functions**

Modulator Design Documentation
System Analysis

Simulink Frequency Domain Simulation Analysis

Modulator Matlab/Simulink Simulation (2nd Order Bandpass)



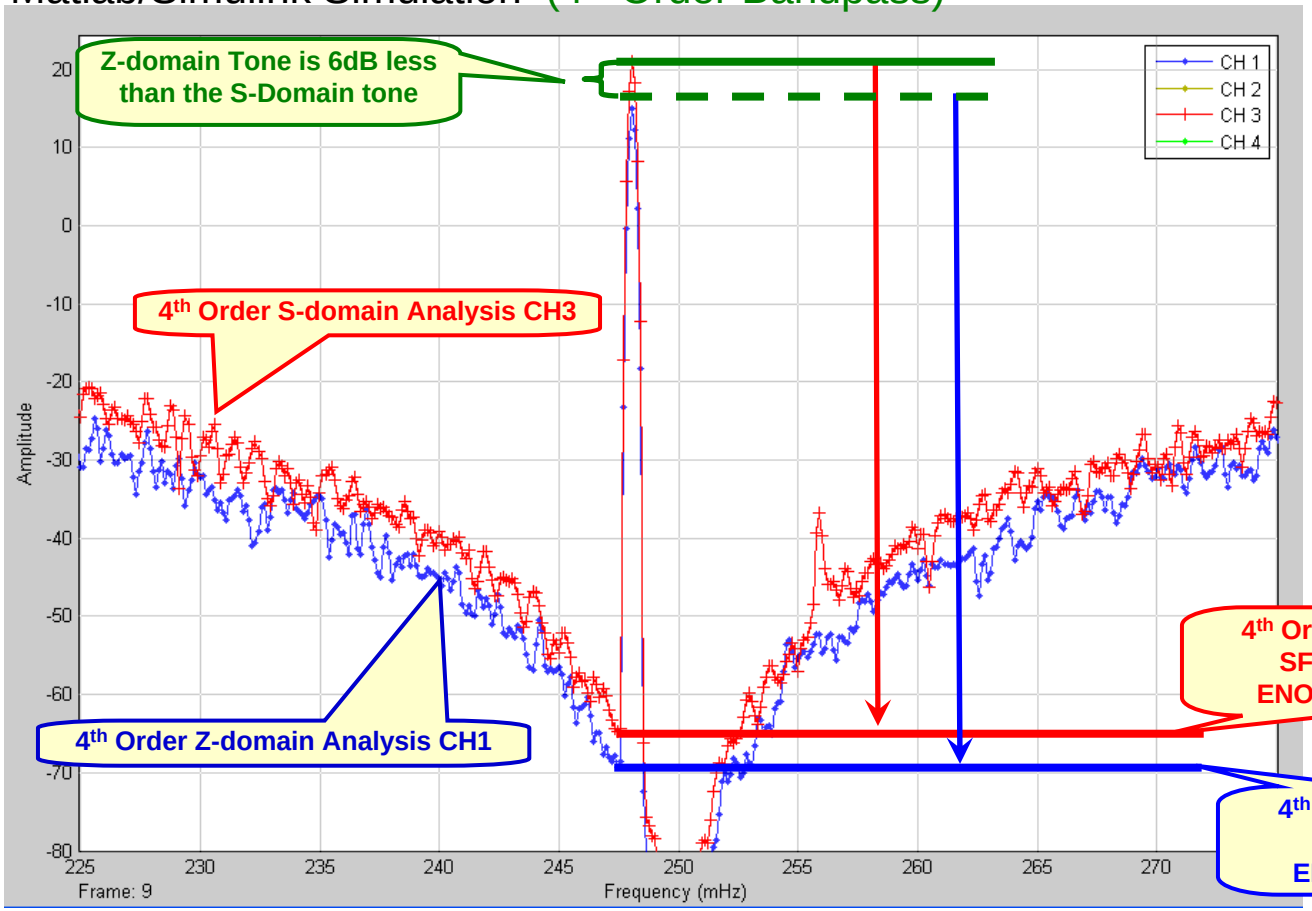
- **The Z-domain loop filter transfer function matches S-domain transfer functions**

Simulink FFT Analysis Results

Modulator Design Documentation
System Analysis

Simulink Frequency Domain Simulation Analysis

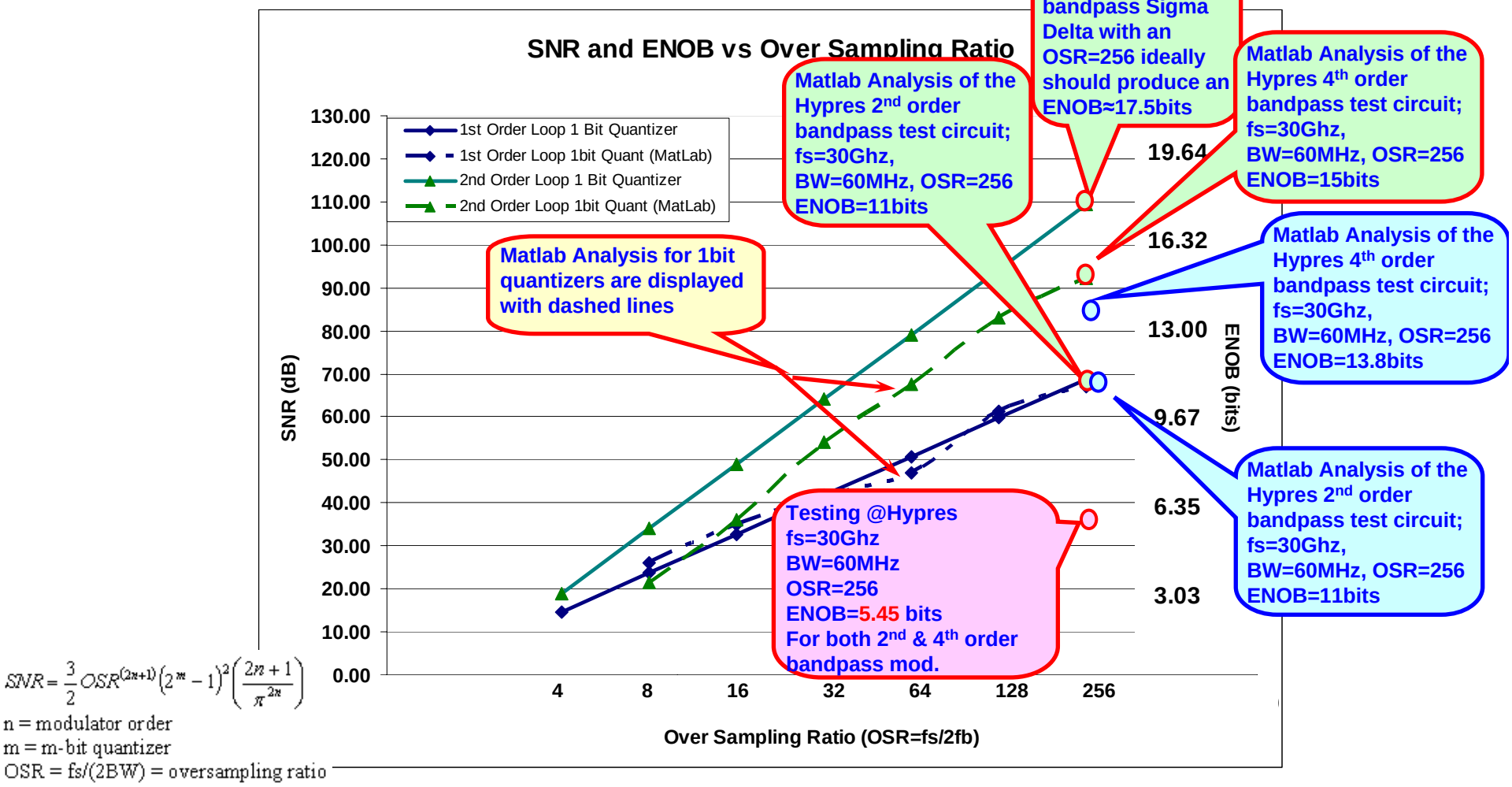
Modulator Matlab/Simulink Simulation (4th Order Bandpass)



- **The Z-domain loop filter transfer function matches S-domain transfer functions**

Simulink FFT Analysis Results

Modulator Design Documentation
Simulated vs Tested Performance
of Modulator Design for this Project



$$SNR = \frac{3}{2} OSR^{(2n+1)} \left(2^m - 1\right)^2 \left(\frac{2n+1}{\pi^{2n}}\right)$$

n = modulator order
m = m-bit quantizer
OSR = fs/(2BW) = oversampling ratio

SNR & ENOB for 2nd & 4th - Order 1-Bit Bandpass Modulators

SNR Equation from:
S. Norsworthy, R. Schreier, and G. Temes, "Delta-Sigma Data Converters: Theory, Design, and Simulation," IEEE Press 1997

Modulator Design Documentation Performance Summary

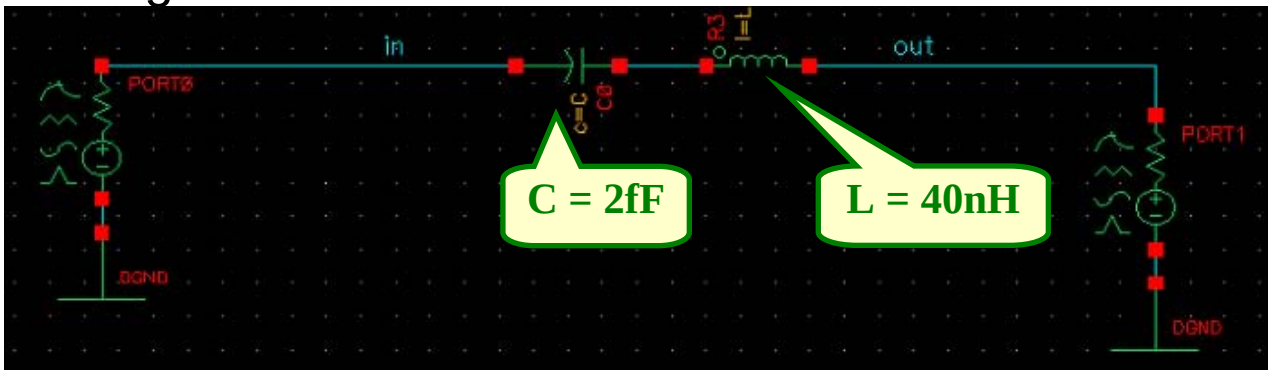
Based on high level Matlab & Simulink simulations the analyzed ADC performance is captured below:

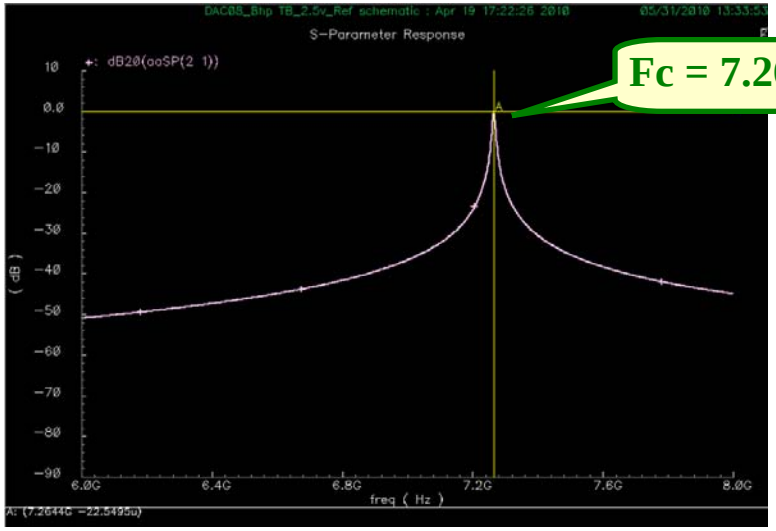
Category			X band RF to Digital ADC			High Level Matlab Simulation		High Level Simulink Simulation	
Item #	ADC Requirement	Units	Device Tested @ Hypres	Project Specification	Project Goal	2nd Order Design	4th Order Design	2nd Order Design	4th Order Design
1	Center Freq. (f_{in})	GHz	7.30	7.30	7.30	7.50	7.50	7.50	7.50
2	Sampling Frequency (Fs, clk)	GHz	29.18	30.00	60.00	30.00	30.00	30.00	30.00
3	Bandwidth (BW)	MHz	57.00	58.59	117.19	58.59	58.59	58.59	58.59
4	Over Sampling Ratio (OSR)		256	256	256	256	256	256	256
5	Physical Bits	bits	1	1	1	1	1	1	1
6	ENOB	bits	5.74	7.74	10	10.42	16.17	11.00	13.83
7	Signal to Integrated Noise And Distortion (SINAD)	dBFS	36.31	48.35	61.96	------	------	------	------
8	Spurs. Free Dynamic Range (SFDR)	dBFS	51.82	60	70	------	------	------	------
9	Signal to Quantization Noise (SQNR)	dBFS	-----	58.35	71.96	64.50	99.10	68.00	85.00

- **Both the Matlab and the Simulink simulations predict the expected performance is well above the project specification.**
- **The analysis is based on an ideal system and only considers quantization noise, however, it does provide a level of confidence that the improvements can be met with this approach.**

Modulator Design Documentation
Resonator Implementation

Resonator Design - Cadence Schematic & Simulation



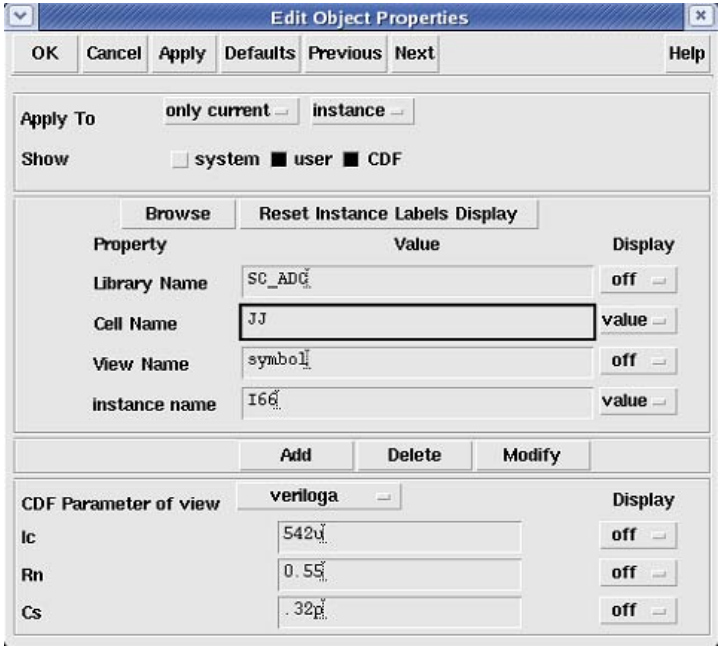


- **Initial center frequency F_c = 7.26GHz**
- **Further design will be performed when the modulator is assembled**

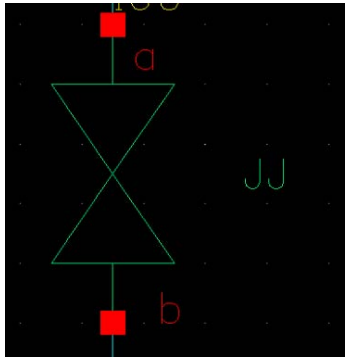
Josephson Junction - Cadence Schematic & Simulation

```
// VerilogA for SC_ADC, JJ, veriloga
// B. Perranoski 5/19/2010

`include "constants.vams"
`include "disciplines.vams"

module JJ (a, b);
inout a, b;
electrical a, b; // access functions are V() and I()
parameter real Ic = 900u;
parameter real Rn = 1;
parameter real Cs = 0.32p;
real I1, I2, I3;
real PI;

   analog begin

   PI = 3.14159265358979323846;


   I1 =  Ic*sin(2.0*PI/2.075e-15*idt(V(a,b)));

   I2 = V(a,b)/Rn;

   I3 = Cs*ddt(V(a,b));

   I(a,b) <+ I1 + I2 + I3;

          end

endmodule
```

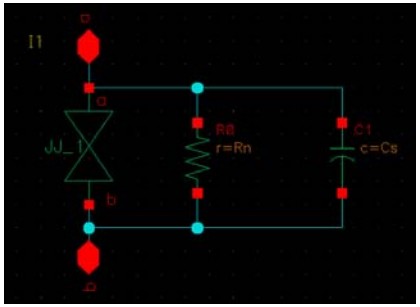
Verilog A Code for RCSJ Josephson Junction Model



Josephson Junction Object Properties: User Input Ic, Rn, Cs overrides the default Verilog A parameters



Josephson Junction Cadence Symbol



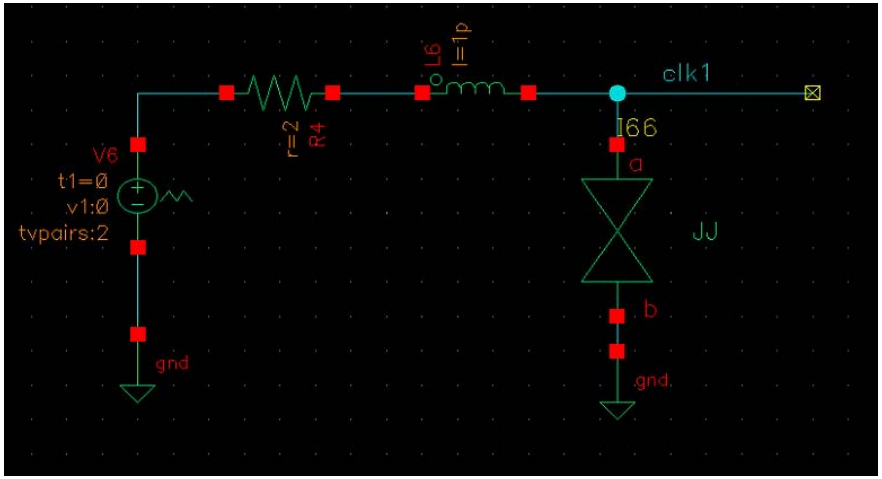
Equivalent Circuit for RCSJ Josephson Junction

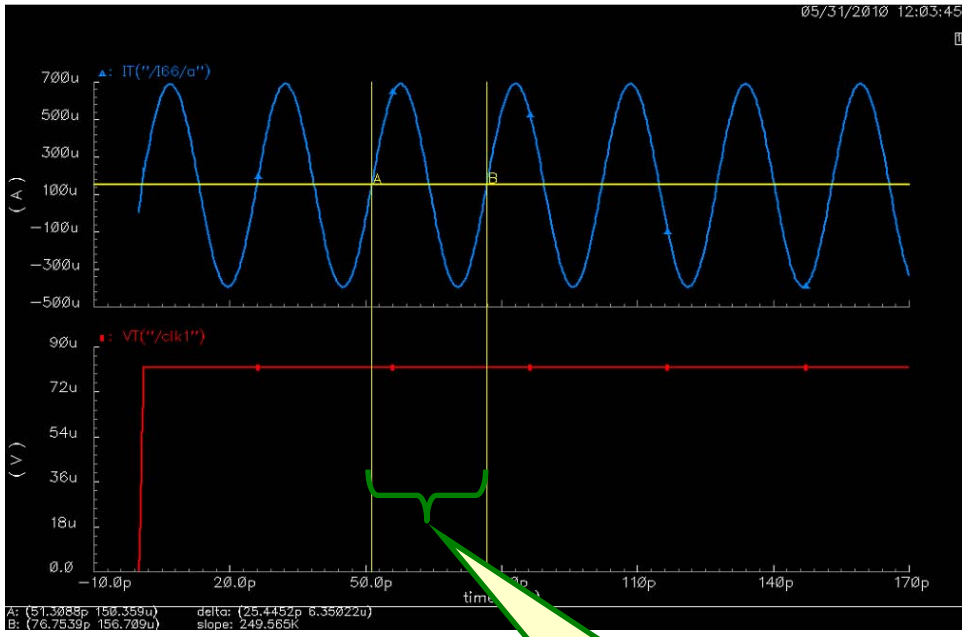
The Josephson Junction RCSJ Model is used for Cadence simulations

The models calculates current through 3 branches.

- **Ideal JJ current = Ic*sin(Φ) = Ic*sin(2π Φ_0*∫Vdt)**
- **Shunt resistor current = V/Rn**
- **Shunt capacitor current = Cs*dV/dt**

Clock Driver Design - Cadence Schematic & Simulation



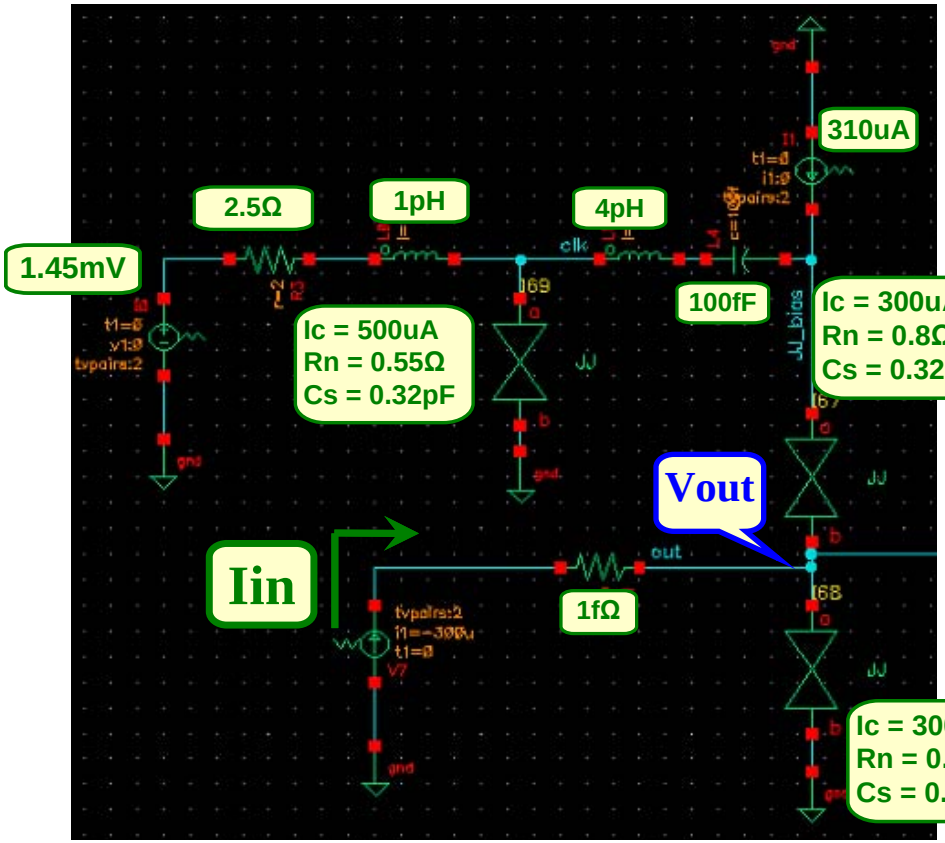


DC Voltage applied across a Josephson junction:
$I = Ic*\sin(\omega_J t)$
$\omega_J = 4\pi eV/h$; $f_J = \omega_J/2\pi = 2eV/h$
For 81.7uV across a junction f_J = 39.3794GHz
Period = 25.4ps

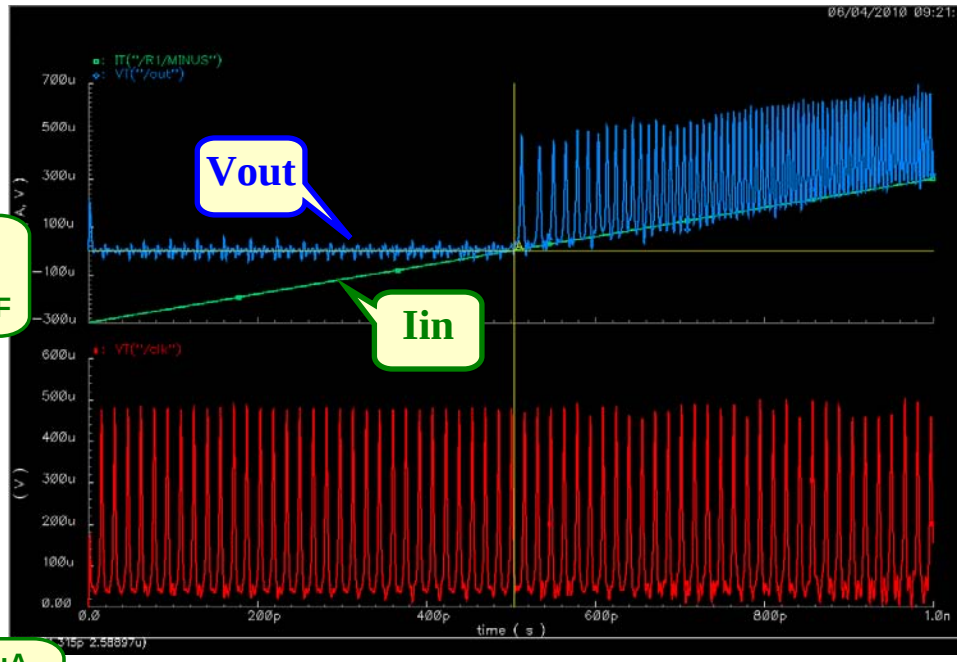
Period = 25.4ps

- **Cadence Simulation Matches Hand Calculations for the Josephson Frequency**

Comparator Design - Cadence Schematic & Simulation

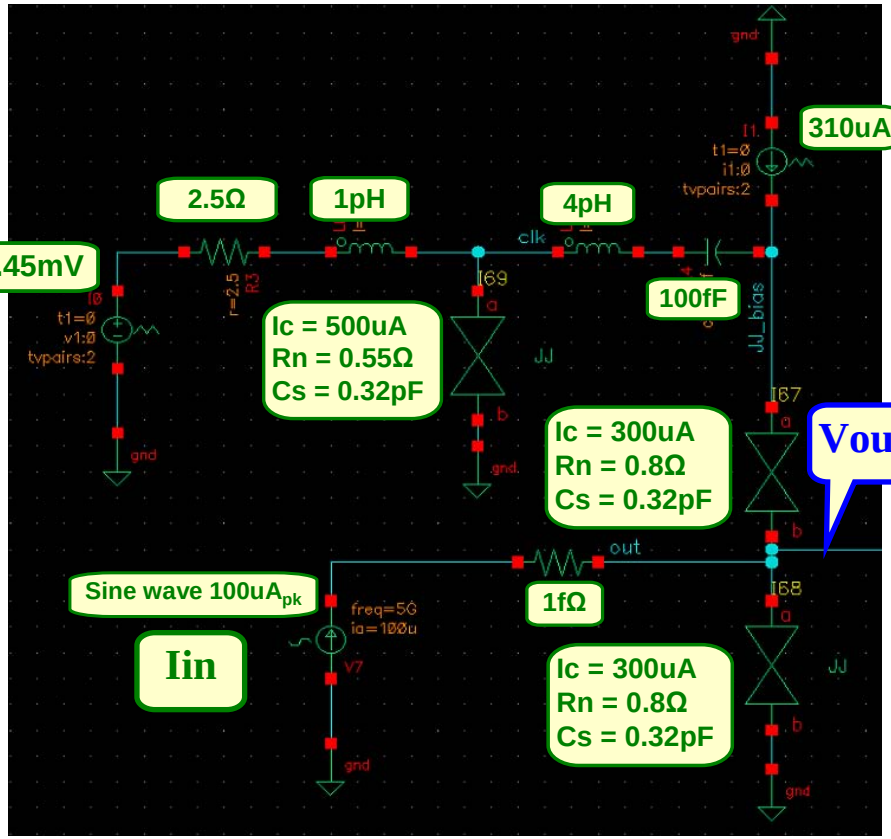


Comparator Testbench

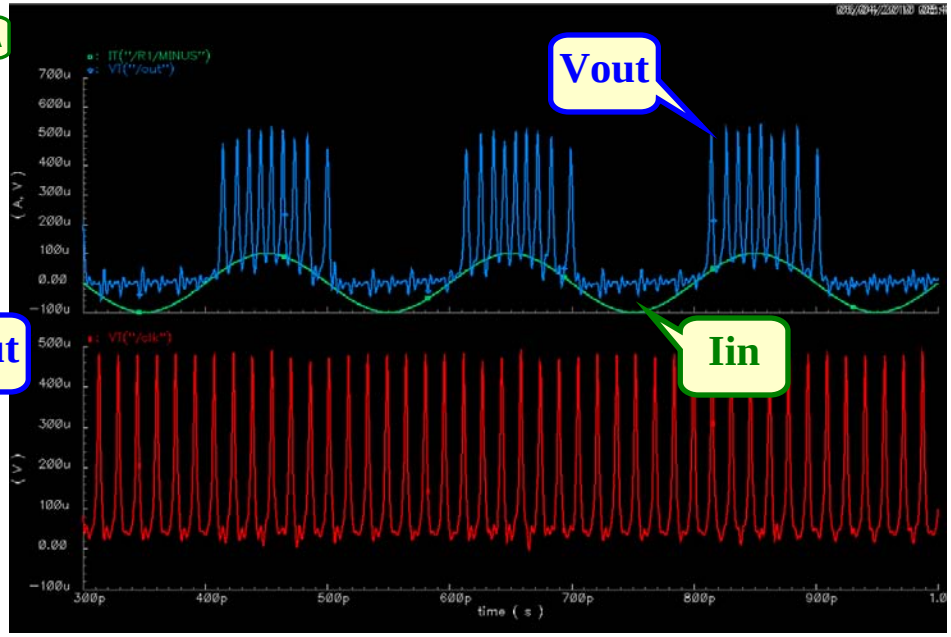


Simulation Results

Comparator Design - Cadence Schematic & Simulation



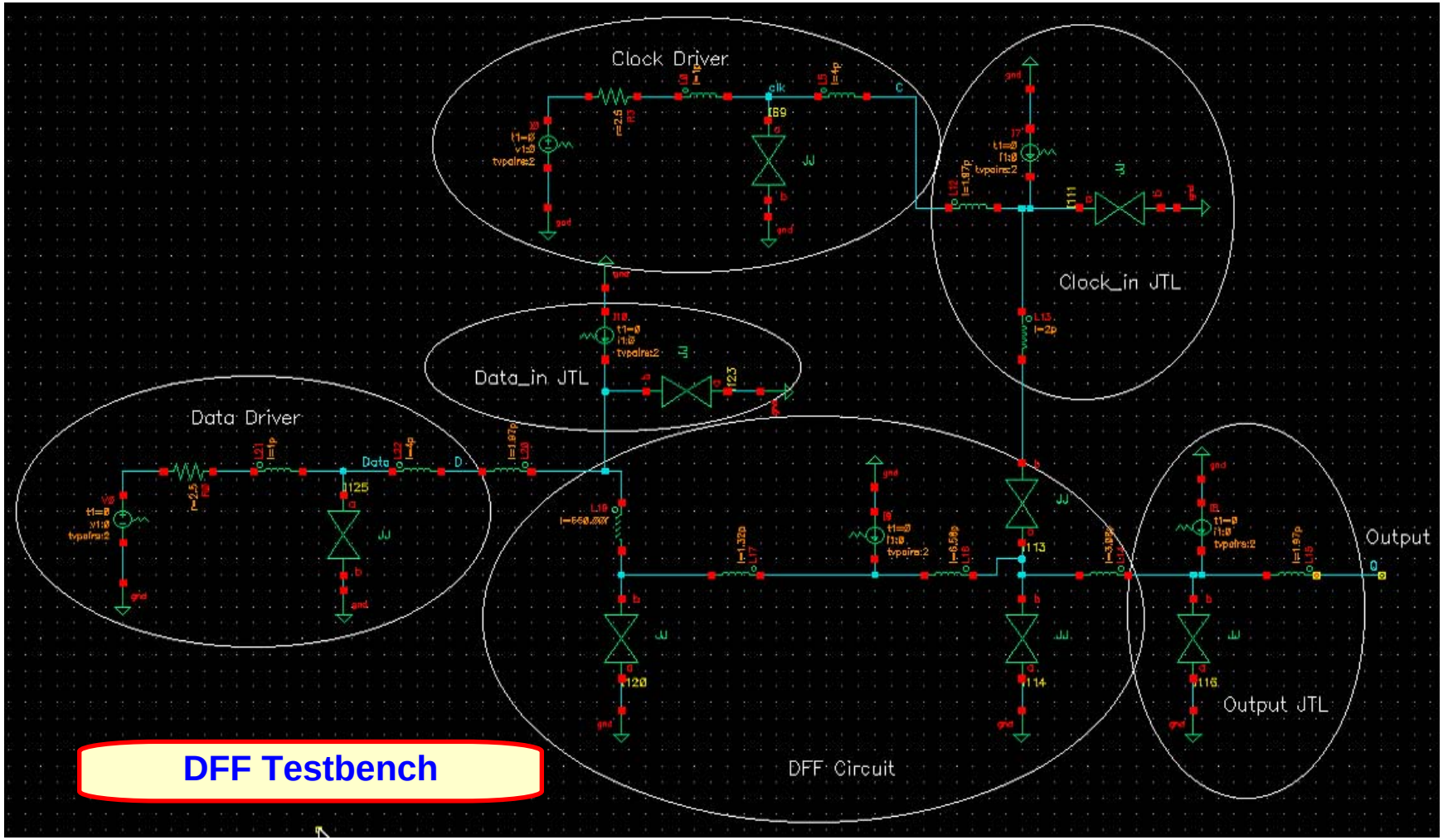
Comparator Testbench



Simulation Results

Modulator Design Documentation
DFF Design

D-Flip Flop Design - Cadence Testbench Schematic



D-Flip Flop Design – Simulation Result

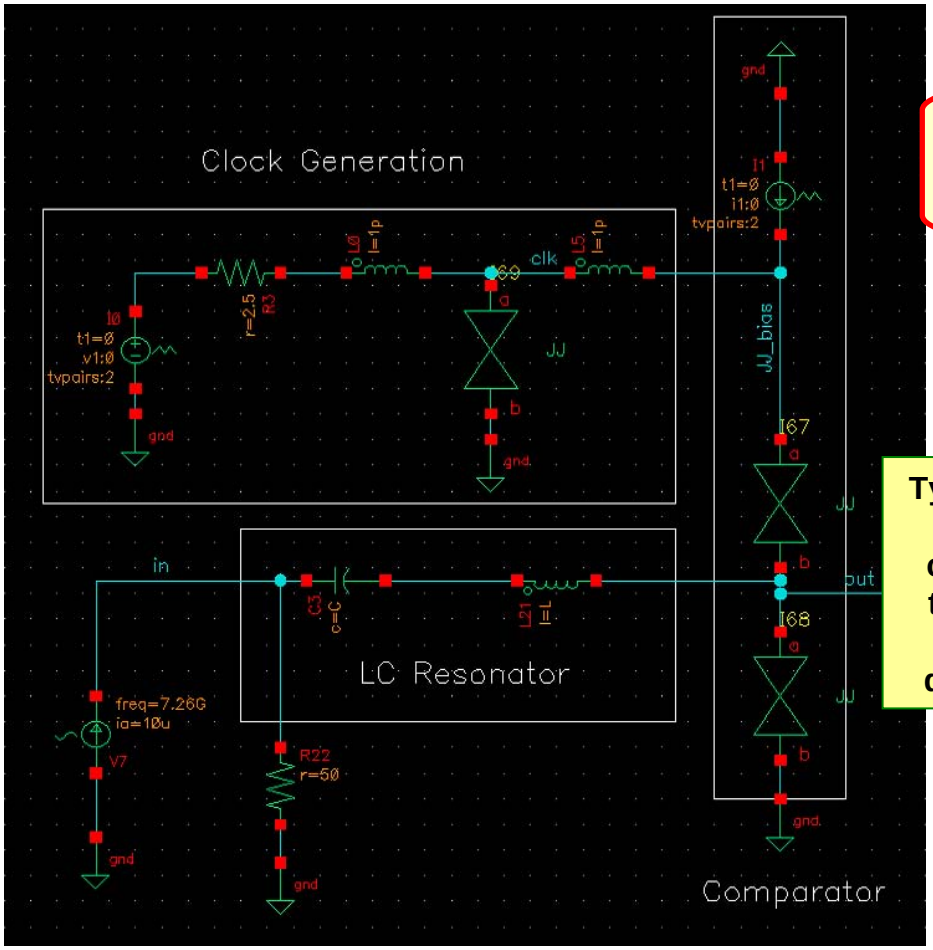
Convergence Issue when simulating the DFF circuit: "Zero diagonal found in Jacobian" Could not simulate the DFF by itself or with other circuitry. This problem has plagued the remaining tasks of this design effort.

/ecad/bigeye_local/Brad_sim/TB_DFF_2/spectre/schematic/psf/spectre.out

File Help 7

```
Zero diagonal found in Jacobian at `I111:idt0' and `I111:idt0'.
Reordering Jacobian.
Zero diagonal found in Jacobian at `I120:idt0' and `I120:idt0'.
Reordering Jacobian.
Trying `homotopy = ptran' for initial conditions..
Trying `homotopy = arclength' for initial conditions.

Error found by spectre during IC analysis, during transient analysis `tran'.
    ERROR (SPECTRE-11005): Matrix is singular (detected at `I125:idt0').
    ERROR (SPECTRE-16080): No DC solution found (no convergence).


The following set of suggestions might help you avoid convergence difficulties.  Once you have a solution, wr

 1. Evaluate and resolve any notice, warning, or error messages.
 2. Perform sanity check on the parameter values using the parameter range checker (use ``+param param-limits

 3. Check the direction of both independent and dependent current sources. Convergence problems might result

 4.  Enable diagnostic messages by setting option `diagnose=yes'.
 5. Small floating resistors connected to high impedance nodes might cause convergence difficulties. Avoid ve
 6. If you have an estimate of what the solution should be, use nodeset statements or a nodeset file and set
 7. Use realistic device models. Check all component parameters, particularly nonlinear device model paramete
 8. If simulating a bipolar analog circuit, ensure the region parameter on all transistors and diodes is set
 9. Loosen tolerances, particularly absolute tolerances like `iabstol' (on options statement). If tolerances
10. Increase the value of gmin (on options statement).
11. Use numeric pivoting in the sparse matrix factorization by setting `pivotdc=yes' (on options statement).
12. Try to simplify the nonlinear component models in order to avoid regions in the model that might contribu
13. Divide the circuit into smaller pieces and simulate them individually, but ensure that the results will b
14. If all else fails, replace the DC analysis with a transient analysis and modify all the independent sourc

Analysis `tran' was terminated prematurely due to an error.
finalTimeOP: writing operating point information to rawfile.

Error found by spectre during DC analysis, during info `finalTimeOP'.
    ERROR (SPECTRE-16041): Analysis was skipped due to inability to compute operating point.

Analysis `finalTimeOP' was terminated prematurely due to an error.
modelParameter: writing model parameter values to rawfile.
element: writing instance parameter values to rawfile.
outputParameter: writing output parameter values to rawfile.
designParamVals: writing netlist parameters to rawfile.
primitives: writing primitives to rawfile.
subckts: writing subcircuits to rawfile.
asserts: writing assert to rawfile.
```

Complete Initial 2nd Order Band-pass Modulator Design Cadence Schematic



The 2nd order sigma delta modulator was able to be simulated without the DFF on the output

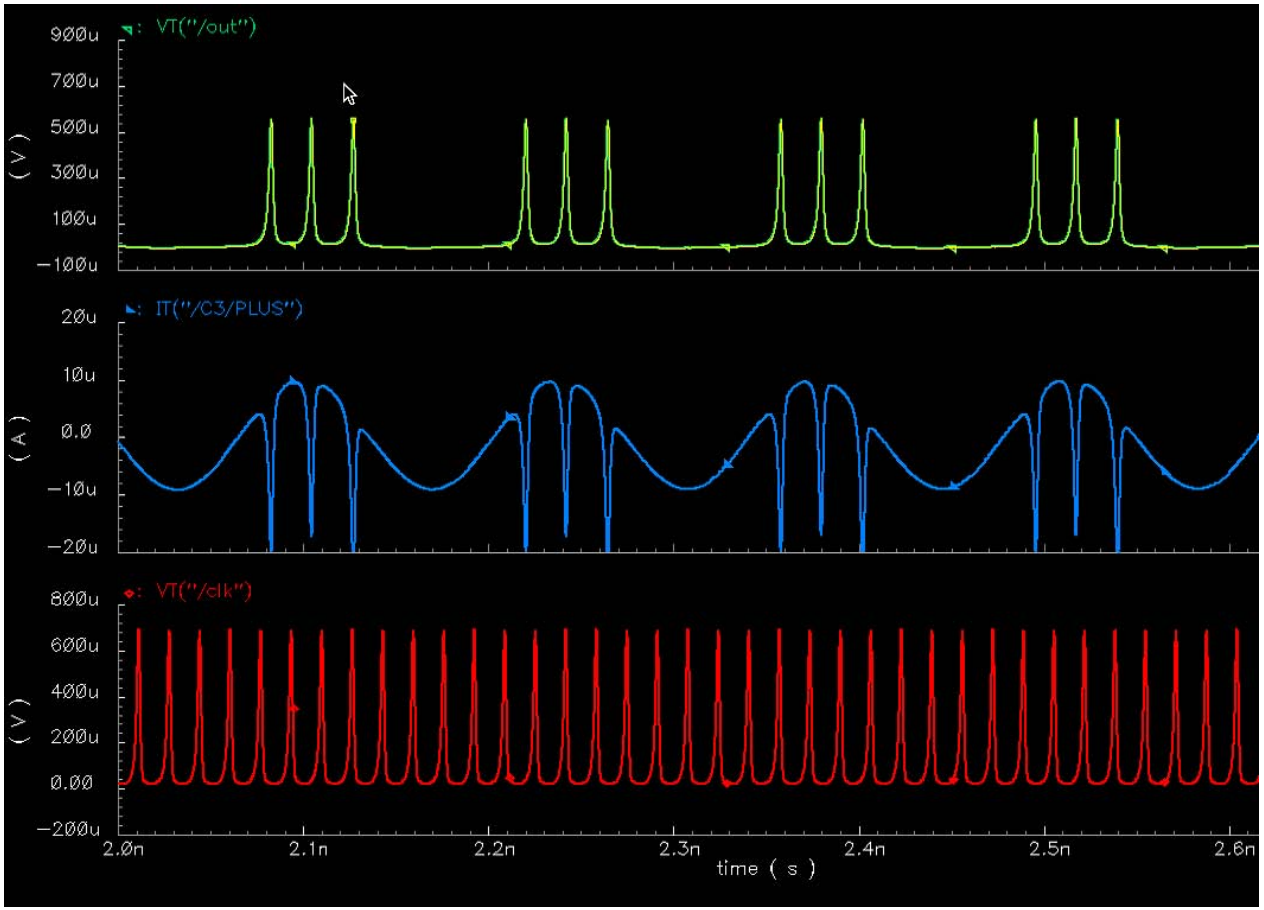
Typically a DFF would be connected to the output to capture the digital pulses

Complete Initial 2nd Order Band-pass Modulator Design Cadence Simulation

Output Voltage (V)

Resonator Input Current (A)

Clock Voltage Pulses (V)



Modulator Design Documentation
Potential ENOB Improvements

Based on the test data gathered earlier in this project, it appears that noise is the limiting factor of the ENOB performance not linearity or SFDR

- **Noise can be broken down into a few components including device noise, thermal noise, and jitter.**
  - **Based on current literature and my own personal observations it appears that jitter is the leading culprit for ENOB degradation in Josephson junction sigma delta ADCs.**
    - **The main source of jitter for this device lies in the comparator gray zone.**
      - **Personal discussions with Thomas Ortlepp and reading his published papers, I believe he has made progress with Josephson junction comparator gray zone improvements.**
        - **Applying his techniques may greatly improve ENOB performance**

Conclusion
What Was Done On This Project

The project consists of 2 phases a Test Phase & a Design Phase

Test Phase

- **Test Plan**
  - **Completed 4/10/2009**
- **Testing**
  - **Completed 5/01/2009 at Hypres in Elmsford, NY**
    - **Test results are documented in the Test Data Review Package submitted 5/18/2009**
- **Data Evaluation**
  - **Completed and submitted to ONR in the Test Data Review Package on 5/18/2009**

Conclusion
What Was Done On This Project (continued)

Design Phase

- **Loop Filter Transfer Function Design (Matlab)**
  - **Completed 9/08/2009 and documented in the Design Review Package submitted 1/11/2010**
    - **Followed a sigma delta design flow to create discrete time (Z-domain) transfer .**
      - **Low pass 1st & 2nd order (both optimized and not)**
      - **Band pass 2nd & 4th order (both optimized and not)**
    - **Converted the Z-Domain transfer functions to a continuous time (S-domain) transfer functions**
      - **Performance simulations were above design goal (4th order >16bits)**
- **Loop Filter Verification (Simulink)**
  - **Completed 1/11/2010 and documented in the Final Design Review Package submitted 1/11/2010**
    - **Used Simulink software to verify that the Z-domain transfer function matched the S-domain transfer function**

Conclusion
What Was Done On This Project (continued)

Design Phase (continued)

- **System Level Modulator Architecture Design (Simulink)**
  - **Completed 3/24/2010 and documented in the Final Design Review Package submitted 6/14/2010**
    - **Simulated both the 2nd & 4th order bandpass sigma delta modulator and compared the Z-domain results with the S-domain results.**
      - **Performance simulations were above design goal (4th order >13bits)**
- **Circuit Level Design**
  - **Resonator Design (schematic)**
    - **Completed 4/20/2010 and documented in the Final Design Review Package submitted 6/14/2010**
      - **Initial schematics & spice level simulations completed**
  - **Comparator Design (schematic)**
    - **Completed 5/25/2010 and documented in the Final Design Review Package submitted 6/14/2010**
      - **Initial schematics & spice level simulations completed**

Conclusion
What Was Done On This Project (continued)

Design Phase (continued)

- **Circuit Design (continued)**
  - **D-Flip Flop (schematic)**
    - **Convergence issued identified when simulating larger circuits**
      - **The Cadence circuit simulator is not designed to handle Josephson junction equations.**
        - **Cadence uses voltages and currents to analyze circuit behavior through Ohms Law or active circuit models (transistors)**
        - **Josephson junctions use the phase difference across the junction to determine the device current. A DC simulation cannot be ran on the Josephson junction circuit.**
        - **A Transient analysis must be ran with a piece-wise-linear PWL voltage or current source with the values starting at 0 and ramping up the desired value. Otherwise the circuit won't converge**
    - **Other simulators like PSCAN or JSIM are designed to perform Josephson junction simulation but are not well developed or are limited in use due to the lack of maturity with the superconductive Integrated circuit technology and design infrastructure**

Conclusion
What Was Done On This Project (continued)

Design Phase (continued)

- **ADC Modulator Design**
  - **The schematic was created for the 2nd order sigma delta modulator and the initial simulations were performed but the progress was limited.**
    - **This effort also contained some of the convergence issues as with the DFF simulations.**
    - **The data is presented in this package (Fabrication Package)**
  - **Due to the convergence issues with the Cadence simulations the 4th order sigma delta schematics were not developed nor were the simulations ran.**
- **Fabrication**
  - **Boeing has determined that the design at this stage will not meet the design goals of the project and recommends not to fabricate the device**

Conclusion (continued)

We Did Not Meet The Goals Of The Project Because:

The goals for this project are to increase the (1) ENOB, (2) discuss the theory behind improvements, (3) document the evolution of the design, and (4) provide further insight into potential ENOB improvements.

Convergence problems with the device level spice simulations were the primary reason for not meeting the first two goals of this project.

This package and the previous three design packages meets the third goal.

The 4th goal is met on the page 22

Conclusion (continued)
This is Where We Are:

- **Top level optimized loop filter transfer functions have been designed & verified for 2nd & 4th order bandpass sigma delta ADC modulators**
- **Modulator architectures has been designed**
- **Initial resonator schematics have been designed and simulated**
- **Initial comparator schematics have been designed and simulated**
- **Initial DFF schematic has been designed, however due to convergence issues I was not able to simulate the DFF**
- **Initial 2nd order bandpass sigma delta ADC modulator schematics have been designed and simulated**
- **The 4th order bandpass sigma delta ADC modulator schematics have not been designed or simulated**
- **No layout has been created for the circuits designed**